

#### EXCEED PROJECT presentation – M18 status

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#### trustEd and fleXible system-on-Chip for EuropEan Defence applications



- The EXCEED project aims at creating a European supply chain of reconfigurable, flexible and trustable programmable system-on-a-chip family targeting a number of ruggedized and secure defence applications
- EXCEED is a project supported by EDA/EC and is running under the <u>Preparatory Action</u> on <u>Defence Research</u>





 The EXCEED consortium encompasses a total of 19 participants from 6 EU countries and Norway.

- Technology providers
- OEMs

EXCEED data

- Certification companies
- The project, which has a duration of **54 months**, will receive an EU grant of roughly €12 million.
- Further information on partners available on the EXCEED project website: <u>www.exceed-padr.com</u>







### EXCEED Objectives (1)



## • A trusted European supply chain based on a European cost effective and reliable technology: the 28nm FDSOI

• The EXCEED project will propose technical solution to avoid constraints brought by non-EU countries domination in SoC/SiPs for Defence applications by designing a European FPGA based System on Chip family suited for European Defence requirements.

#### • To achieve this objective, the EXCEED project will:

- Define a comprehensive set of requirements and specifications for SoC/SiP devices and related supply chain that considers the military specificities about operating environment, content protection, compliance with EU and National classified information and the various mission profiles.
- Develop a first prototype and get it tested by OEMs (Original Equipment Manufacturers).
- Develop synergies and supply chains with other European critical sectors such as Space, Aeronautics and Industrial.
- Assess the gaps to be fulfilled to overcome the dependence on non-EU technology providers and propose a roadmap for the creation of a trusted European supply chain.





#### **EXCEED Objectives (2)**



• The EXCEED workplan structure will follow the steps below:





#### **EXCEED** impacts



- The project is targeting the following impacts
  - Ensure secure and autonomous availability of high performance and trustable (re)configurable SoC/SiPs to military end-users.
  - Contribute to strengthening the European microelectronics industry and help improve its global position through the implementation of innovative technologies along a new European manufacturing value chain.
  - Demonstrate the potential of EU-funded research in support of EU critical defence technologies, in particular in the domain of (re)configurable SoC/SiPs.







# Main achievements after 18 months

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### Achievements @M18



- Use cases requirements fully specified (from security and technical points of view)
- SoC architecture defined
- Lifecycle management needs specified (SoC in systems)
- Softwares toolchain defined, based on end-users' requirements
- Augmented toolchain roadmap delivered
- Design started
- Trusted SiP studies activities started







#### Targeted use cases



### Tactical Systems and devices use cases

- Military Radios
- Electronics Devices for
   Dismounted Soldiers
- On-ground signal processor for real- time COMINT
- Unified real-time Homeland
   Tactical Situation
- EW digital receiver

#### Security use cases

- Encryption devices
- Secure PNT applications
- Secure communications among distributed sensors

### Airborne embedded computing use cases

- Weapon control in missile systems
- Embedded applications of launcher avionics
- Seekers and sighting applications





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#### EXCEED trusted/secure SoCs Key Features

- **<u>Programmable processing</u>:** dual core APU A53 (Linux OS support), Dual core RTP R52
- **Configurable processing:** field programmable capabilities e.g. LUT, DSP, DPRAM
- <u>Security</u>: secure boot, crypto accelerators, OTP key storage, TRN generator, Lifecycle management
- <u>Connectivity</u>: e.g., Legacy/high speed connectivity, programmable Direct/Complex I/O
- Others: red / black separation, Developed with FDSOI 28nm for low power, leading to a family of SoCs to support all Use Cases requested and identified requirements

64 bits + 8 bits ECC						
Processing System	Processing System Memory Controllers DDR3/4 SDRAM eMMC host (NAND) QSPI (NOR) Connectivity					
Trace Port	ARM CoreSight Debug & Trace			PCle (x2)		
Secure Unit Secure CPU Secure boot Crypto services Boot & Service QSPI NOR SpaceWire Spl slave Protection Unit	Platform Mgnt Unit 200 MHz+ ARM <sup>®</sup> Cortex <sup>TM</sup> -M23 ROM (64 kB) RAM (128 kB) System Reg GPIO UART	Application Processing Unit 1.0 - 1.4 GHz ARM <sup>®</sup> Cortex <sup>TM</sup> -A53 32kB L1 NEON <sup>TM</sup> MMU FPU GIC 1 MB L2 Cache	Real-Time Processing Unit Split & 600 MHz ARM® Cortex <sup>TM</sup> -R52 32kB L1 NEON <sup>TM</sup> MPU FPU GIC 128 kB TCM (x3)	GbEth (x2) SpaceWire (x2) SPI (x4) UART (x4) I2C (x4) GPIOs		
Bitstream Manager CoreLink™ NIC-400 Network Interconnect						
System         SMU         Watchdog         Timers         Error Manager         VTSENS         OMUX         Mailbox         OTP         DMA (x2)         Fabric Interface         2 MB ECC on-chip RAM						
FPGA Fabric		High Speed Connective HSSL Comple	ty General C	Connectivity		
19x24 Mult. Preadder 56 bits ALU	True Dual Port 48 kbits 36 kbits w/EDAC	12.5 Gbps SpaceFibre JESD2048 ESIstream SRIO	1.8V to 3.3V	1.8V to 3.3V		
				Programmable Logic		





#### Use cases vs SoC architecture



	Use Case	SoC Subsystems			
1	Secure Software Defined Radio				
2	IP Encryptors				
3	Use of Trusted, re-Configurable Soc/Sip in Secure PNT Applications				
4	Electronic Devices for Dismounted Soldier				
5	Secure Communication among Distributed Sensors				
6	On Ground, Signal Processor for Real-time Comms Intelligence				
7	Unified Real-rime Homeland Tactical Situation				
8	WEAPON CONTROL IN MISSILE SYSTEMS				
9	Evaluation of Flexibility, Real-time, Performance And Reliability for Embedded Applications of Launcher Avionics				
10	Seekers and Sighting Applications				
11	1       Signal Processing and de-Interleaving Algorithm Implementation in EW Digital Reception				
LEG	SECURE SUBSYSTEM GENERAL PURPOSE SUBSYSTEM REAL-TIME SUBSYSTEM	PROGRAMMABLE LOGIC SUBSYSTEM			
	SYSTEM FUNCTION EXTERNAL MEMORY CONTROLLERS SUBSYSTEM PLATFORM MANAGEMENT SUBSYSTEM	I I/O CONNECTIVITY SUBSYSTEM			



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